REMARKS/ARGUMENTS

Claims 1-17 are pending in the application. Claims 1-17 are rejected. Claim 9 has been amended.

As requested by the Examiner, the applicants have presented and filed any reference(s) known to qualify as prior art.

Claims 1-17 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-30 of copending application No. 10/231,414. Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. §102(e) as being anticipated by Chiu et al. ("Chiu") U.S. Patent Application 2002/01994429. Claims 5, 13, and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chiu in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp. 140-240 ("Handy"). Claims 16-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chiu in view of Handy in further view of Witt et al. ("Witt") U.S. Patent No. 6,202,139. Alternatively, Claims 1-15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lee et al. ("Lee") U.S. Patent 6,477,621 in view of Handy. Claims 16-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Handy in further view of Witt.

Provisional Double-Patenting Rejection

A terminal disclaimer regarding copending application No. 10/231,414 has been filed along with the present response.

Claim Rejections under 35 U.S.C. §102

Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. §102(e) as being unpatentable over Chiu. Chiu discloses a method, apparatus, article of manufacture, and a memory structure that provides high availability cache coherency in a distributed cache environment for a storage cluster. (*See* block 17).

Applicants respectfully submit that Chiu does not disclose a plurality of sub-unit caches, each assigned to one of said plurality of storage nodes, as recited in claim 1, 6, and 9 as amended. Chiu states:

> A cluster storage subsystem 100 is comprised of one or more hosts 102 in a host storage area network 104, *a number of cache storage nodes 106-08 in a storage cluster* 116, and one or more storage disks 110 in a device storage area network 112. The hosts 102 view the storage cluster 116 as a *single logical image of storage*. Further, hosts 102 can connect to the cluster 116 through *any* storage node 106-108.

(Chiu, block 33).

Further, all of the storage nodes 106-108 have a direct access path to *any* disk 110.

(Chiu, block 34).

In other words, Chiu does not require that the storage nodes each be coupled to one of a plurality of storage disks, but instead the storage nodes can access *any* disk attached to the device storage area network. Thus, because each cache resides on a separate storage node, and each storage node can access *any* disk, each cache is not assigned to one of said plurality of storage disks.

Therefore, claims 1, 6, and 9, are not anticipated by Chiu. Accordingly, reconsideration and withdrawal of the rejection of claims 1, 6, and 9 under 35 U.S.C. §102(e) is respectfully requested. In addition, Applicants respectfully submit that claims 2-4, 7-8, 10-12 and 14 are

allowable as depending from allowable base claims 1, 6 and 9.

Claim Rejections under 35 U.S.C. §103

Claims 5, 13, and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chiu in view of Handy. Handy discloses a protocol for use in multiple processor system with multiple caches.

As discussed above, Chiu does not disclose a plurality of sub-unit caches, each assigned to one of said plurality of port components as recited in claim 1 and claim 9 as amended, and by their dependency claims 5, 13, and 15. Handy does not disclose a plurality of sub-unit caches, each assigned to one of said plurality of port components. Therefore, Applicants respectfully submit that claims 5, 13, and 15 are allowable as depending from allowable base claims 1 and 9 given the arguments above.

Claims 16-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chiu in view of Handy and in further view of Witt. Witt discloses a pipelined data cache with multiple ports. The invention of Witt is described as a computer system including a processor having a cache that includes multiple ports. The cache is pipelined and operates at a clock frequency higher than that employed by the remainder of the microprocessor including the cache for multiple accesses per clock cycle. (*See* Abstract, Summary of the Invention, col. 2, lines 31-36).

As discussed above, neither Chiu nor Handy discloses a plurality of sub-unit caches, each assigned to one of said plurality of port components as recited in claim 9 as amended, and by their dependency claims 16-17. Witt does not disclose a plurality of sub-unit caches, each assigned to one of said plurality of port components. Therefore, Applicants respectfully submit

that claims 16-17 are allowable as depending from allowable base claim 9 given the arguments above.

Alternatively, the Office Action rejects claims 1-15 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Handy and rejects claims 16-17 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of Handy and further in view of Witt. Lee discloses a memory system having a main memory which is coupled to a plurality of parallel virtual access channels. Each of the virtual access channels provides a set of memory access resources for controlling the main memory. These memory access resources include cache resources. (*See* Abstract).

As discussed above, Handy does not disclose a plurality of sub-unit caches, each assigned to one of said plurality of port components. Applicants respectfully submit that Lee does not disclose a plurality of sub-unit caches, each assigned to one of said plurality of port components, as recited in claims 1, 6 and in claim 9 as amended. The Office Action argues that the channel row cache interface circuits 501-507 are each coupled to one of a plurality of bank row interface circuits 401-404. Lee states:

> FIG. 3 is a block diagram of a memory system 300 in accordance with one embodiment of the present invention. Memory system 300 includes memory banks 301-304, bank row interface circuits 401-404, memory bank interface bus 310, virtual channel system 320, memory system interface bus 312, memory system interface 314 and system bus 315. Memory system interface 314 is coupled to one or more external memory masters (not shown) through the system bus 315.
>
> The virtual channel system 320 includes memory bank interface bus 310, channel row cache interface circuits 501-507, channel row cache memories 601-607, cache row address registers 701-707, channel row cache interface circuits 801-807, bus bypass circuit 311, memory system interface bus 312, and virtual channel control circuit 325.

(Lee, column 4, lines 43-57)

In other words, the channel row cache interface circuits 501-507 are not coupled to one of a plurality of bank row interface circuits 401-404, but are instead each linked to the bank row interface circuits 401-404 through the single memory bank interface bus 310. The plurality of channel row cache memories 601-607 are not each assigned to one of said plurality of bank row interface circuits 401-404 because, as noted above, the plurality of channel row cache interface circuits 501-507 to which the plurality of channel row cache memories 601-607 are coupled, interfaces with the bank row interface circuits 401-404 through the single memory bank interface bus 310. Indeed, the design calls for fewer bank row interface circuits 401-404 than channel row cache memories 601-607. Therefore, Applicants respectfully submit that claims 2-5, 7-8, and 10-15 are allowable as depending from allowable base claims 1, 6 and 9 given the arguments above.

As discussed above, neither Lee nor Handy discloses a plurality of sub-unit caches, each assigned to one of said plurality of port components as recited in claims 9 as amended, and by their dependency claims 16-17. Witt does not disclose a plurality of sub-unit caches, each assigned to one of said plurality of port components. Therefore, Applicants respectfully submit that claims 16-17 are allowable as depending from allowable base claim 9 given the arguments above.

Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 1-17 under 35 U.S.C. §103(a) is respectfully requested.

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon, deposit account no. **11-0600**.

Respectfully submitted,

KENYON & KENYON

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By: Stephen T. Neal
Stephen T. Neal
(Reg. No. 47,815)
Attorneys for Intel Corporation

KENYON & KENYON
333 West San Carlos St., Suite 600
San Jose, CA 95110

Telephone: (408) 975-7500
Facsimile: (408) 975-7501